PATENT

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PATENT APPLICATION

METHOD OF FORMING ROUNDED CORNER IN TRENCH

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METHOD OF FORMING ROUNDED CORNER IN TRENCH

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority from R.O.C. Patent Application No. 092115751, filed June 10, 2003, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a method for forming rounded corners in the trench, and more particularly to a method of forming rounded corners in the trench of trench-type Metal-Oxide Semiconductor (trench-type MOS) devices or other integrated circuit elements.

[0003] Nowadays, trench-type MOS devices are widely used in the semiconductor industry. Figs. 1(a) and 1(b) are diagrams illustrating part of a conventional fabrication method of the trench-type MOS devices. As shown in Fig. 1(a), in the manufacturing process of trench-type Metal-Oxide Semiconductor Field Effect Transistor (MOSFET), a semiconductor substrate 10 is firstly provided, and a pad oxide layer 11, a silicon nitride layer 12 and an oxide layer 13 are formed sequentially on the semiconductor substrate 10. Then, the oxide layer 13, the silicon nitride layer 12, the pad oxide layer 11 and the semiconductor substrate 10 are removed partially to form at least one trench 14 on the semiconductor substrate 10 with a conventional process, for example, the photolithography or etching process.

[0004] Because of the plasma etching process used for forming the trench 14, some lattice defects or non-planar surfaces are usually formed simultaneously on the sidewalls of the trench 14. As a result, in order to solve this problem, a sacrifice oxide layer (not shown) is first formed on the trench 14 and then removed later.

[0005] Then, as shown in Fig. 1(b), an oxide layer is formed on the oxide layer 13 and in the trench 14 to be a gate oxide layer or dielectric layer 15. After that, some processes, such as the formation of a bottom oxide layer (not shown) at the bottom of the trench 14 and/or the deposition of a polysilicon layer into the trench 14, will be further performed to complete the manufacturing process of the trench-type Metal-Oxide Semiconductor Field Effect Transistor (MOSFET).

[0006] As seen in Fig. 1(a), after the trench 14 is formed by the plasma etching process, the sidewalls of the trench 14 usually have a vertical profile, and the bottom corner of the trench forms nearly a right angle. Therefore, during the subsequent oxidation processes, a gate oxide layer or a dielectric layer 15 would be formed along the entire profile of the trench 14. After the subsequent oxidation processes, a polysilicon layer may be deposited in the trench 14 which is formed by first removing the oxide layer 13, the silicon nitride layer 12, and the pad oxide layer, with the top corners and the bottom corners of the trench 14 each nearly at a right angle. As a result, the lattices of the polysilicon near the top corners of the trench 14 would squeeze each other to apply corner stresses on the top corners of the trench 14. Moreover, the gate oxide layer or the dielectric layer 15 near the bottom corners of the trench 14 also would be formed with non-uniform thickness.

[0007] Figs. 2(a) and 2(b) are scanning electron microscope (SEM) pictures of the top corners and bottom corners of the trench through the steps of the conventional manufacturing process. As illustrated in Fig. 2(a), the top corners of the trench 14 each have the profile of substantially a right angle. Thus, the lattices near the top corners of the trench 14 would squeeze each other. It leads to corner stresses in the trench 14. Therefore, point discharge would occur when a trench type MOSFET is operated. In addition, as shown in Fig. 2(b), the bottom corners of the trench 14 are not rounded, but are each at substantially a right angle. The thickness of the gate oxide layer or the dielectric layer 15 will be non-uniform when the gate oxide layer or the dielectric layer 15 is formed in the trench 14. This could cause serious current leakage when the trench type MOSFET is operated.

BRIEF SUMMARY OF THE INVENTION

[0008] Embodiments of the present invention provide a method for forming rounded corners in the trench, which is used for manufacturing trench-type Metal-Oxide Semiconductor (MOS) devices or integrated circuit elements to prevent or reduce corner stress and non-uniform thickness of gate oxide layer or dielectric oxide layer and further to prevent or reduce the occurrence of point discharge and current leakage of semiconductor devices.

[0009] In accordance with an aspect of the present invention, a method for forming a trench having rounded corners in a semiconductor device comprises providing a semiconductor substrate; forming a first pad oxide layer, a first silicon nitride layer, and a

first oxide layer on the semiconductor substrate sequentially; removing portions of the first oxide layer, the first silicon nitride layer, the first pad oxide layer, and the semiconductor substrate to form at least one trench; and removing portions of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer in the trench above an upper corner of the semiconductor substrate in the trench. The semiconductor substrate includes a lower corner at a bottom of the trench. The method further comprises forming a second pad oxide layer in the trench; forming a second silicon nitride layer on the second pad oxide layer and the first oxide layer; removing portions of the second silicon nitride layer to expose the second pad oxide layer on the corners and the bottom of the trench; forming a thermal oxide layer on the second pad oxide layer exposed by removing the portions of the second nitride layer; and removing the second silicon nitride layer, the thermal oxide layer, and the second pad oxide layer.

[0010] In some embodiments, removing portions of the first oxide layer, the first silicon nitride layer, the first oxide layer, and the semiconductor substrate is performed by a photolithography process or an etching process. At least one trench has a depth of between about 1μm and about 3μm and a width of about 0.2μm and about 1μm. Removing portions of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer in the trench is performed using HF. The second silicon nitride layer is formed by deposition. Removing portions of the second silicon nitride layer to expose the second pad oxide layer is performed by dry etching. The thermal oxide layer is formed by thermal oxidation. Removing the second nitride layer, the thermal oxide layer, and the second pad oxide layer is performed with phosphoric acid. The method may further comprise forming a second oxide layer in the trench and on the first oxide layer after removing the second silicon nitride layer, the thermal oxide layer, and the second pad oxide layer. The second pad oxide layer is formed over surfaces of the semiconductor substrate in the trench. Removing portions of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer in the trench exposes the upper corner of the semiconductor substrate in the trench. Removing the second silicon nitride layer, the thermal oxide layer, and the second pad oxide layer forms a rounded upper corner and a rounded lower corner of the semiconductor substrate in the trench for a trench-type metal oxide semiconductor device.

[0011] In accordance with another aspect of the invention, a method for forming a trench having rounded corners in a semiconductor device comprises providing a

semiconductor substrate having thereon a first pad oxide layer, a first silicon nitride layer on the first pad oxide layer, and a first oxide layer on the first silicon nitride layer, and at least one trench extending through the first oxide layer, the first silicon nitride layer, and the first pad oxide layer, and partially through the semiconductor substrate. The trench is enlarged above the semiconductor substrate along sidewalls of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer. The semiconductor substrate includes a lower corner at a bottom of the trench and an upper corner below the sidewalls of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer. The method further comprises forming a second pad oxide layer in the trench; forming a second silicon nitride layer on the second pad oxide layer and the first oxide layer; removing portions of the second silicon nitride layer to expose the second pad oxide layer on the corners and the bottom of the trench; forming a thermal oxide layer on the second pad oxide layer exposed by removing the portions of the second nitride layer; and removing the second silicon nitride layer, the thermal oxide layer and the second pad oxide layer.

[0012] In accordance with another aspect of the present invention, a method for forming a trench having rounded corners in a semiconductor device comprises providing a semiconductor substrate having thereon a first pad oxide layer, a first silicon nitride layer on the first pad oxide layer, and a first oxide layer on the first silicon nitride layer, and at least one trench extending through the first oxide layer, the first silicon nitride layer, and the first pad oxide layer, and partially through the semiconductor substrate. The trench is enlarged above the semiconductor substrate along sidewalls of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer. The semiconductor substrate includes a lower corner at a bottom of the trench and an upper corner below the sidewalls of the first oxide layer, the first silicon nitride layer, and the first pad oxide layer. A second pad oxide layer is formed in the trench and a second silicon nitride layer is formed on the second pad oxide layer and the first oxide layer. The method further comprises removing portions of the second silicon nitride layer to expose the second pad oxide layer on the corners and the bottom of the trench; forming a thermal oxide layer on the second pad oxide layer exposed by removing the portions of the second nitride layer; and removing the second silicon nitride layer, the thermal oxide layer and the second pad oxide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figs. 1(a) to 1(b) are diagrams illustrating part of a conventional fabrication method of the trench-type MOS devices.

[0014] Fig. 2(a) is a scanning electron microscope (SEM) picture from the top of the trench through the conventional fabrication.

[0015] Fig. 2(b) is a scanning electron microscope (SEM) picture from the bottom of the trench through the conventional fabrication.

[0016] Figs. 3(a) to 3(g) are diagrams illustrating process steps according to an embodiment of the present invention.

[0017] Fig. 4(a) is a scanning electron microscope (SEM) picture from the top of the trench through the fabrication of the present invention.

[0018] Fig. 4(b) is a scanning electron microscope (SEM) picture from the bottom of the trench through the fabrication of a semiconductor device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] The method of the present embodiment is primarily applied to manufacture a trench-type Metal-Oxide Semiconductor (trench-type MOS) device or an integrated circuit element with rounded corners in the trench, to prevent or reduce corner stress and non-uniform thickness of gate oxide layer and dielectric oxide layer, further to prevent or reduce the occurrence of point discharge and current leakage, and to prevent or reduce the change of the electrical properties of the trench-type MOS or integrated circuit element. Although the present embodiment takes the fabrication of the trench-type Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) as an example, other types of trench-type power MOS devices can utilize the method of the invention.

[0020] Figs. 3(a) to 3(g) are the diagrams illustrating the exemplary embodiment of present the invention. As shown in Fig. 3(a), in the fabrication process of the trench-type Metal-Oxide Semiconductor Field Effect Transistor (MOSFET), a semiconductor substrate 20 is first provided, and the semiconductor substrate 20 is usually a silicon substrate. Then, a pad oxide layer 21, a silicon nitride layer 22 and an oxide layer 23 are formed sequentially on the semiconductor substrate 20, wherein the first pad oxide layer

21 serves as a buffer for lowering the stress between the semiconductor substrate 20 and the first silicon nitride layer 22, and the first oxide layer 23 is a silicon oxide layer. After that, the first oxide layer 23, the first silicon nitride layer 22, the first pad oxide layer 21 and the semiconductor substrate 20 are removed partially by the photolithography or etching process to form at least one trench 24. Preferably, the trench has a depth of between about 1.0μm and 3.0μm and a width of between about 0.2μm and 1.0μm.

[0021] Then, as shown in Fig. 3(b), the first oxide layer 23, the first silicon nitride layer 22, and the first pad oxide layer 21 near the trench 24 are removed partially by a wet etching process with HF. After that, as shown in Fig. 3(c), a second pad oxide layer 25 is formed on the trench 24, and a second silicon nitride layer 26 is deposited on the second pad oxide layer 25 and covers the first oxide layer 23. Preferably, the second pad oxide layer 25 has a depth of between about 300Å and 400Å, and the second silicon nitride layer 26 has a depth of about 200Å.

[0022] As shown in Fig. 3(d), the second silicon nitride layer 26 is removed in the horizontal direction (X direction) with a dry etching process. After that, the second silicon nitride layer 26 in vertical direction (Y direction) will remain, so as to expose the second pad oxide layer 25 on the top corners of the trench 24 and the bottom of the trench 24 and the first oxide layer 23. Next, as shown in Fig. 3(e), a thermal oxide layer 27 is formed by thermal oxidation process on the top corners and the bottom of the trench 24 exposed by etching the second silicon nitride layer 26 in the preceding step. At the same time, a thin thermal oxide layer 27 is also formed on the first oxide layer 23. After that, as shown in Fig. 3(f), the second silicon nitride layer 26, the thermal oxide layer 27, and the second pad oxide layer 25 are removed by HF to form the trench 24 with top rounded corners and bottom rounded corners. Finally, as shown in Fig. 3(g), a second oxide layer is formed on the trench 24 and the first oxide layer 23 to be a gate oxide layer or dielectric layer 28.

[0023] Then, the following steps may be performed to finish the manufacturing process. For example, a bottom gate oxide layer is formed on the bottom of the trench 24, polysilicon is deposited in the trench 24, and/or the first oxide layer 23, the first silicon nitride layer 22, and the first pad oxide layer 21 are removed to finish the fabrication of MOSFET.

[0024] Figs. 4(a) and 4(b) are scanning electron microscope (SEM) pictures of the top and bottom corners, respectively, of the trench manufactured according to the present

embodiment. As illustrated in Fig. 4(a), the top corners of the trench 24 each have a substantially rounded profile using the above-mentioned process. Therefore, the lattices near the top corners will not squeeze each other easily, and the corner stress will not form as readily in the trench as in the prior art. The point discharge will be avoided or reduced when the trench type MOSFET device is operated. Furthermore, as shown in Fig. 4(b), the bottom corners of the trench 24 each have a substantially rounded profile using the above method. As a result, the thickness of the gate oxide layer or dielectric layer 28 will be formed more uniformly, so that serious current leakage, will be prevented when trench-type MOS device is operated.

[0025] In sum, the present embodiment provides a method for forming rounded corners in the trench as applied to a trench-type Metal-Oxide Semiconductor (trench-type MOS) device or in the fabrication of other integrated circuits. Through the present method, not only the problems of the corner stress and the non-uniform thickness of the gate oxide layer, but also the occurrence of point discharge and current leakage, can be avoided or reduced.

[0026] The above-described arrangements of apparatus and methods are merely illustrative of applications of the principles of this invention and many other embodiments and modifications may be made without departing from the spirit and scope of the invention as defined in the claims. For example, the shapes and sizes of the components that form the camera supporting device may be changed. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.